A 10-bits pipeline ADC dedicated to the VFE Electronics of Si-W Ecal

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A 10-bits pipeline Analog-to-Digital Converter (ADC) has been designed in a 0.35 μm CMOS technology and prototypes tested. This ADC is a building block of the very-front-end electronics dedicated to the Si-W electromagnetic calorimeter. Based on a 1.5-bit resolution per stage architecture, it reaches the 10-bits precision at a sampling rate of 4 MSamples/s with a consumption of 35 mW. Integral and Differential Non-Linearity measured never exceed respectively $\pm$1 LSB and $\pm$0.6 LSB over the 2V dynamic range, with a level of noise limited to 0.47 LSB at 68% C.L.

1 Introduction

The very-front-end readout electronics of the Si-W Electromagnetic Calorimeter (ECAL) of ILC has to process 10^8 channels which deliver a 15-bits dynamic range signal with a precision of 8 bits. Moreover, the minimal cooling available for the embedded readout electronics imposed an ultra-low power limited to 25 μW per channel. This issue will be reached thanks to the timing of ILC which allows the implementation of a power pulsing with a duty ratio of 1%. A key component of the very-front-end electronics is the Analog-to-Digital Converter (ADC) which has to reach a precision of 10 bits. In order to save the die surface of the chip and to limit the power consumption, one ADC will be shared by several channels. To fullfill this request, an ADC operating at a sampling rate of the order of one MSamples/s has been designed and tested.

2 Description of the pipeline ADC

The ADC designed is based on a pipeline architecture [**?**]. A resolution of 2 bits per stage has been chosen in order to attenuate the contributions to the non-linearity of the gain error and of the offset voltages. As the two output bits of each stage are combined with the next one and the combination"11" avoided, the effective resolution per stage is 1.5 bit [**?**]. This 1.5-bit/stage pipeline ADC architecture [**?**] involves two comparators per stage, with separate threshold voltages V_{Th}^{Low} and V_{Th}^{High}, and two reference voltages V_{Ref}^{Low} and V_{Ref}^{High}. A 2-bits word $[b_2 b_1]_i$ is delivered by each stage i.
The global schematic of one ADC stage with resolution of 2 bits is given on Fig. **??**. In order to reject the common mode noise, a fully differential structure has been adopted. As represented on Fig. **??**, the value of the reference signal added to the $(V_{In})_i$ input signal is selected by comparators outputs through switches. Then the circuit operates on two clock phases: during the sampling phase, the input signal and the reference signal are summed through capacitors 2C, while during the hold phase, the summed signal is amplified by factor 2. The gain-2 amplifier is built with a differential amplifier and a capacitive feedbacked loop. A better matching is obtained with capacitors and they have been preferred to resistors.

This matching is particularly important because it affects the precision of the gain 2, and therefore, the linearity of the ADC. Thus, feedback capacitors must be large enough to minimize both the thermal noise kT/C and the components mismatch proportional to $1/\sqrt{C}$. In contrast, both the small die surface and the dynamical performance achieved with low supply current have to be carry out. Then capacitors values of 300 fF and 600 fF are used.

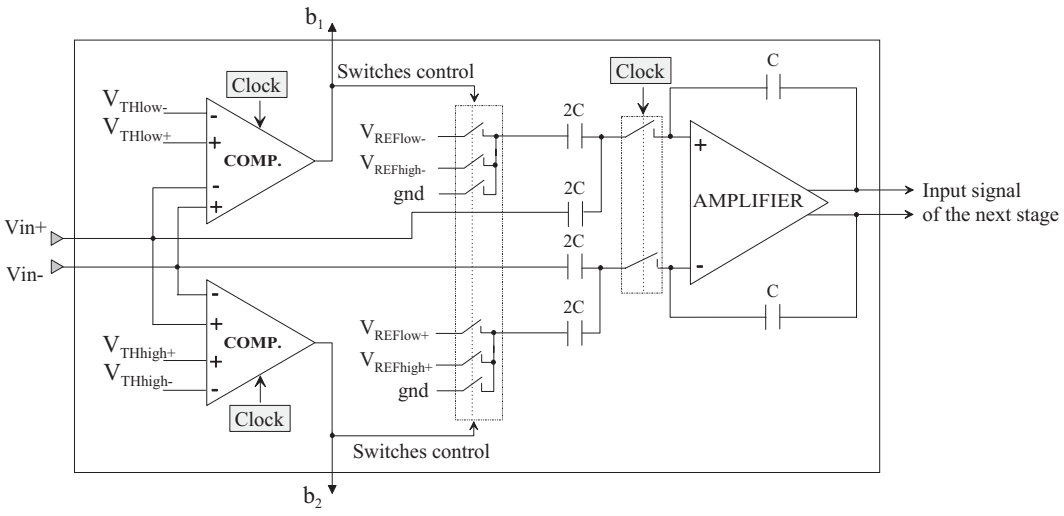

Figure 1: Simplified schematic of one ADC stage: 2 comparators give the output bits of the stage and determine the reference signals substracted to the input signal; the amplifier amplifies by a factor 2 the redidual voltage and delivers it to the next stage.

3 Measurement Results

Architecture	1.5-bit/stage
Technology	0.35μm 2-P 4-M CMOS
Area	1.5 mm x 0.9 mm
Supply Voltage	0-5 V
Resolution	10 bits
Full scale	2 V differential
Sample rate	4 MS/s
Consumption	35 mW @ 4 MHz
INL	+0.85/-0.70 LSB
DNL	+0.56/-0.46 LSB
Noise	0.47 LSB @ 68% C.L.
Gain Error	0.8% of full scale
Zero Error	0.5% of full scale

Table 1: Summarized performance of the pipeline ADC.

A 10-bits ADC prototype has been fabricated using the Austriamicrosystems 0.35 μm 2-poly 4-metal CMOS process. The total area of the ADC is 1.35 mm^2 and the chip is bounded into a JLCC 44 pins package. The circuit is measured with a 5.0 V supply and a differential input swing of 2.0 V_{pp}, at a frequency clock of 4 MHz.

Main performance is reported on table **??**. A dynamic input range of 2.0 V is measured with zero and gain errors respectively of 5 LSB and 8 LSB. The standard deviation of the noise is lower than 0.5 LSB at 68% C.L.

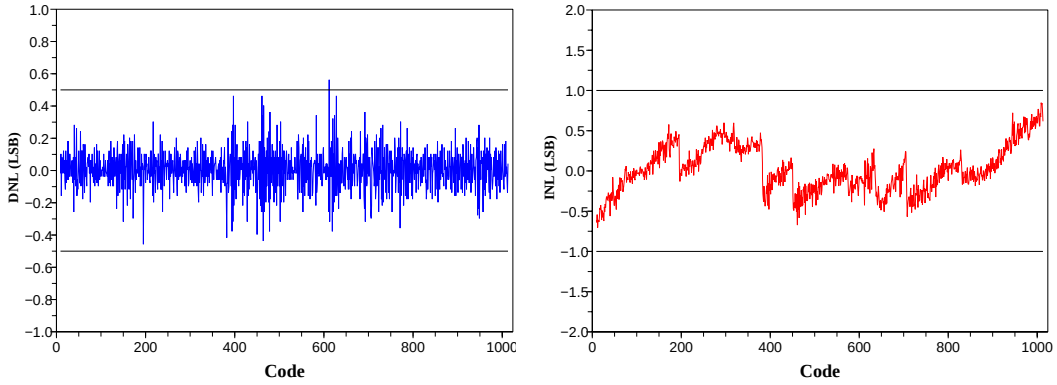

Figure 2: Differential (left) and integral (right) nonlinearity measurements

The static linearity curves of the 1.5-bit/stage ADC are given in Fig. **??**. The Differential Non-Linearity (DNL) is defined as the difference between an actual step width and the ideal value of one LSB. The DNL measured is within a ± 0.6 LSB range. The Integral Non-Linearity (INL) refers to the deviation, in LSB, of each individual output code from the ideal transfert-function value. The INL curve plotted in Fig. **??** never exceeds +0.85/-0.70 LSB over the 2V dynamic range.

At a sampling rate of 4 Msamples/s the dissipation of the chip is 35 mW. With a time of 250 ns to convert one analogue signal and considering the number of events stored per channel to be less than 5, the power consumption integrated during the ILC duty cycle of 200 ms is evaluated to $0.22\,\mu W$/channel. Assuming that the ON-setting time and the pipeline latency of the convertion are neglected when the ADC is shared by tens of channels, the integrated power dissipation of the ADC is then limited to 1 % of the total power available for the very front-end electronics of the ECAL.

4 Conclusion

A 10-bit 4-MSamples/s 35-mW CMOS ADC based on a pipeline 1.5-bit/stage architecture has been designed and tested. Its performance confirms that this architecture fullfill the ADC requirements of the ECAL at ILC. Bearing in mind that the comsumption is a key point, the next step will consist on a portage in 3V supply.

References

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